

FCDN614-UBM

1-Channel ESD Protector

Functional Description

The FCDN614-UBM provides robust ESD protection for sensitive parts that may be subjected to electrostatic discharge (ESD). The tiny form factor and single wirebond requirement enables it to be used in very confined spaces. The electrical 'back-to-back Zener' configuration also provides ESD protection in cases where nodes with AC signals are present. This device is designed and characterized to safely dissipate ESD strikes of at least ± 8 kV, according to the MIL-STD-883 (Method 3015) specification for Human Body Model (HBM) ESD.

Features

- Compact Die Protects from ESD Discharges
- Almost No Conduction at Signal Amplitudes Less than ± 4 V
- ESD Protection to over ± 8 kV Contact Discharge per MIL_STD_883 International ESD Standard

Applications

- LED Lighting
- Modules
- Interface Circuits

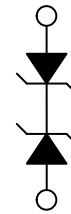


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ELECTRICAL SCHEMATIC

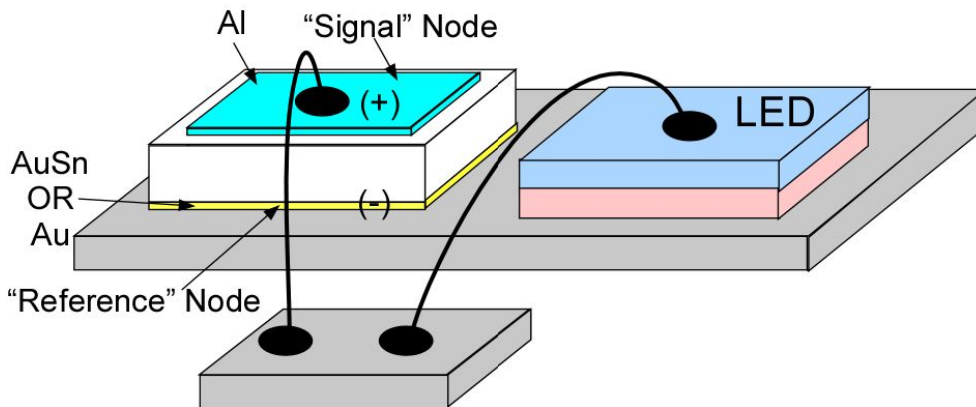
Al (Aluminum on Underside)



Bare Silicon on Underside

ORDERING INFORMATION

For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.



NOTE: The diagram shows a typical application with an AuSn or Au back metal on the ESD die. The diagram also shows the polarity convention for the ESD die.

Figure 1. Applications Drawing

FCDN614-UBM

Table 1. CURRENT/VOLTAGE GRAPH

Symbol	Description
I_{CL+}	Positive Clamping Current
V_{CL+}	Positive Clamping Voltage
I_{L2+}	Leakage Current at V_{L2+}
V_{L2+}	Voltage Condition: +10 V
I_{L1+}	Leakage Current at V_{L1+}
V_{L1+}	Voltage Condition: +4 V
I_{CL-}	Negative Clamping Current
V_{CL-}	Negative Clamping Voltage
I_{L1-}	Leakage Current at V_{L1-}
V_{L1-}	Voltage Condition: -4 V

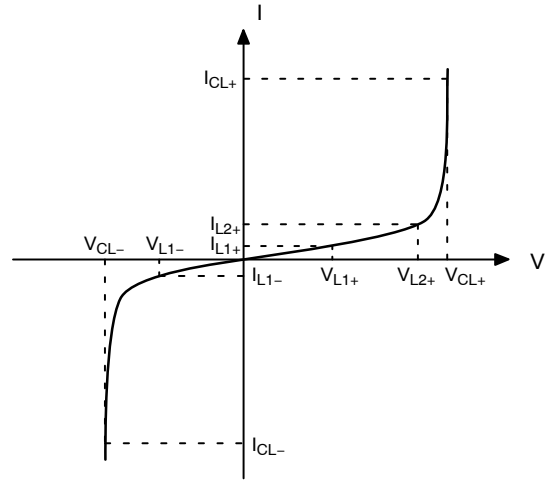


Figure 2. Current/Voltage Graph

Table 2. ORDERING INFORMATION

Ordering Part Number	Topside Metal	Backside Metal	Thickness	Shipping Method
FCDN614-UBM	Al (Aluminum)	Bare Silicon	4 mils	Wafer Form

SPECIFICATIONS

Table 3. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
Operating Temperature Range	-40 to +150	°C
Storage Temperature Range	-65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 4. STANDARD OPERATING CONDITIONS

Parameter	Rating	Units
Operating Temperature Range	-40 to +150	°C

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SPECIFICATIONS (Cont'd)

Table 5. ELECTRICAL CHARACTERISTICS (Note 1)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{LEAK}	Leakage Current	$V = \pm 4\text{ V}$, 150°C (Note 2) $V = \pm 4\text{ V}$, 25°C ($V_{L1\pm}$) $V = +10\text{ V}$, 25°C (V_{L2+})			4.0 0.3 ($I_{L1\pm}$) 0.5 (I_{L2+})	mA μA μA
V_{CL}	Signal Clamp Voltage Positive Polarity on Signal Node (V_{CL+}) Negative Polarity on Signal Node (V_{CL-})	$T_A = 25^\circ\text{C}$ at 10 mA (I_{CL+}) at -10 mA (I_{CL-})	+10.5 -9.0	+12.0 -7.0	+15.0 -5.0	V
V_{ESD}	ESD Protection – Withstand Voltage: Human Body Model (MIL-STD-883, Method 3015)	$T_A = 25^\circ\text{C}$ (Note 2)	± 8			kV
V_{CL_ESD}	Clamping Voltage during Transient Events on Signal Node	$I_{PP} = 1\text{ A}$, $t_P = 8/20\ \mu\text{s}$ Positive Transients Negative Transients (Note 2)		+22 -15		V
C_{IN}	Input Capacitance	At 1 MHz, 30 mV osc. Level, 0 VDC Bias At 1 MHz, 30 mV osc. Level, 3 VDC Bias (Note 2)		4.7 3.0		pF

- Operating characteristics are over standard operating conditions unless otherwise specified.
- This parameter is guaranteed by design and/or characterization.

MECHANICAL DETAILS

Table 6. MECHANICAL SPECIFICATIONS

Parameter	Condition	Units
Composition	Silicon Wafer, p+ Doped	
Die Shape	Square	
Length (Stepping Size)	240	μm
Width (Stepping Size)	240	μm
Thickness	4	mils
Saw Street Widths (Space between Devices on Wafer) (Note 1)	70 (X-Direction) 70 (Y-Direction)	μm
Top Pad Length	125	μm
Top Pad Width	125	μm
Top Pad Composition	Al (Aluminum)	
Back Metal (Underside)	Bare Silicon	
Die (Stepping Size)	240	μm
Passivation Opening	70	μm
Active Size	160	μm
Active to PA Opening	5	μm

- The saw street is defined as the passivation-free area between devices.

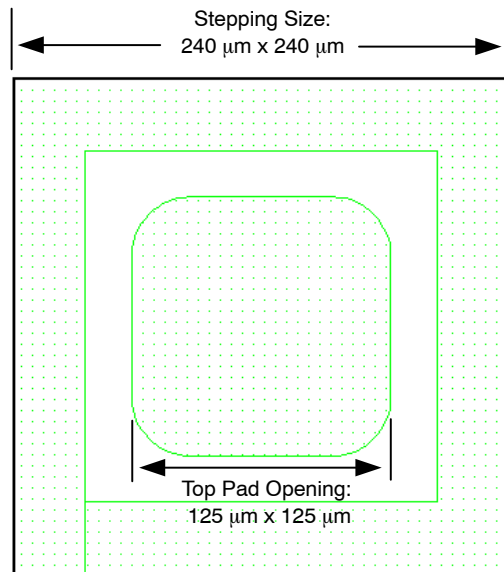


Figure 3. Package Dimensions

FCDN614-UBM

MECHANICAL DETAILS (Cont'd)

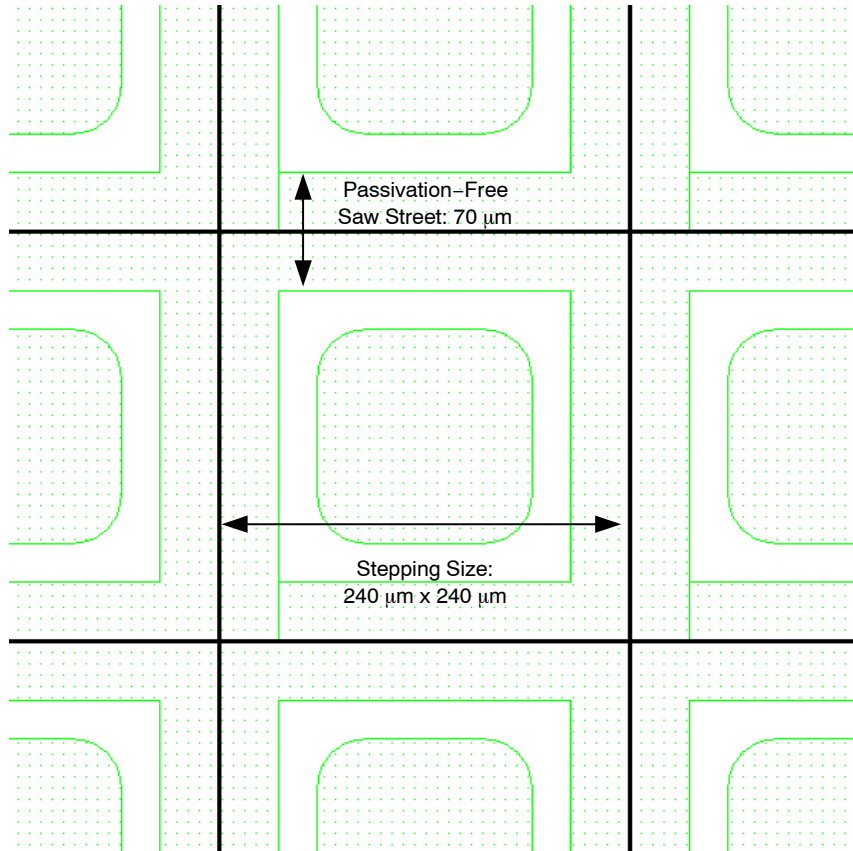


Figure 4. Wafer Array

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